FBE ASIC Design & Consulting

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F-CSA104

4-Channel CMOS Low-Noise Charge Sensitive Preamplifier

General Description

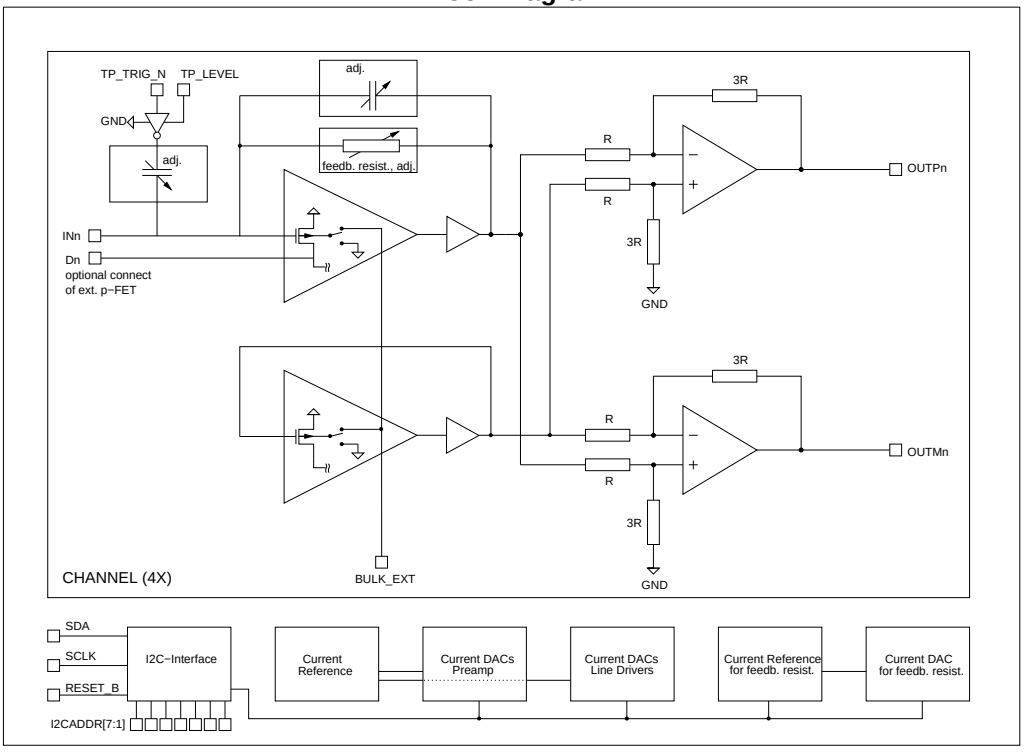
F-CSA104 contains 4 channels of charge sensitive preamplifiers with differential line drivers. It has particularly been designed for the use with semiconductor detectors operating with liquid nitrogen as coolant (T = 77K/-196°C) .
F-CSA104 joins the formerly discrete input FET with the preamplifier in a single IC, thus forming the next step of integration for better immunity to interference.
F-CSA104's noise performance has been optimized for use with capacitive detectors of 0 - 100pF; flicker noise is reduced by use of a p-channel MOSFET as input transistor. In cases where noise matching to higher capacitance detectors is vital, an external p-channel FET may be connected to the IC.
A range of F-CSA104's parameters (including offset and preamplifier decay constant) can be programmed by I^2C commands. F-CSA104's linearity and offset have been designed for use with 14 bit ADC systems, thus being ideally suited for spectroscopy applications.

The high current drive differential line drivers allow for directly driving a 100 Ohm twisted pair cable.

Features

- Very low noise (ENC=220e$^-$ @ C_{det} = 30pF, T=27°, T_{peak} = 20µs)
- Temperature range -200°C ... +50°C
- Fast differential outputs (t_{rise} < 30 ns)
- Gain 5.84 mV/fC, 316 mV/MeV(Ge), 258mV/MeV(Si)
- Input signal range ± 600 fC, ± 11MeV(Ge), ± 13MeV(Si)
- 14 bit linearity for spectroscopy applications
- Adjustable preamplifier time constant 1us ... 1.5ms
- Optional connection of external p-channel FET
- Optimized for detectors of 0 pF ... 100 pF
- All stages DC coupled, triple offset suppression
- I^2C-interface for parameter adjustment

Block Diagram



Preamplifier

Charge delivered by a semiconductor detector is collected and amplified by the charge sensitive preamplifier (Fig. 1). Its output voltage Vout is given by

Vout = Q / Cfb

where Q is the charge delivered to the input and Cfb is the feedback capacitance (1 pF after calibration).

The preamplifier has been optimized for noise, speed, and open loop gain. The noise performance is completely determined by the input PMOS (PMOS has been selected over NMOS because of its lower flicker noise) which matches best to detectors with capacitances of 0 - 100pF (see Fig 7). If larger detector capacitances are used and noise perfomance is critical, one (or several) external FETs may replace the internal PMOS (see section "External p-channel FET"). Speed, to some extent, comes automatically by the input transistor's large transconductance but must also be supported by the preamplifier's buffer stages. Open loop gain is critical for minimization of charge collection deficit and impact of the detector's capacitance on the amplification. Open loop gain is not easily achieved since the signal current generated by the input transistor would be "swallowed" immediately by its low drain-source-resistance if not special precautions had been taken.

Several parameters can be adjusted via I^2C commands. The BULK_HI bit of the MODE[8:1] byte controls whether the input transistor's bulk is connected to GND (default) or to external pad BULK_EXT. The bulk voltage Vbulk must be clean from noise and voltage interference since the bulk terminal has a finite (albeit small) transconductance similiarly to the gate terminal. The intrinsic bulk resistance noise can be reduced if V(BULK_EXT) is made higher than the source voltage GND (V(BULK_EXT) ≤ +3V). If there is a clean and stable VDDA line, BULK_EXT could be connected to VDDA. If no appropriate voltage is available, GND should be used. The SEL_EXT bit of the MODE[8:1] byte allows for connection of an external FET to replace the internal PMOS (see section "External p-channel FET"). INP[5:1] controls the DC current flowing in the input PMOS. At default settings, the operation current is 1mA.

PA[5:1] controls the other currents flowing in the preamplifer (the default setting should not have to be modified).

The NO_OFF bit of the MODE[8:1] byte allows for connection of depletion-type FETs (further described in section "External p-channel FET").

For subtraction of offset and common mode noise, a reference (dummy) preamplifer controlled by the same bias settings is used within each channel. It uses a down-scaled version of the input transistor running at a likewise down-scaled current. A remaining offset may be further reduced by settings OFFP[5:1] and OFFN[5:1] which act on the reference amplifier's output voltage by adding or subtracting current to the level shifting MOS diode. More details about the offset supression concept can be found in section “Offset supression”.

Feedback Capacitor

In the CMOS process used, capacitors suffer from an absolute variance of ±11%. Variation of the feedback capacitor affects particularly the preamplifier's gain. Thus, the feedback capacitor has been designed as an adjustable weighted capacitor array (Fig. 2) . The user may decide to adjust the effective feedback capacitor using register CFB[5:1] (Formula 1 behind Table 2).

An absolute calibration should not be executed with the internal test pulse generator which uses a capacitor suffering from the same variation, but by using charge pulses from a detector or by feeding a voltage step to an external capacitor.

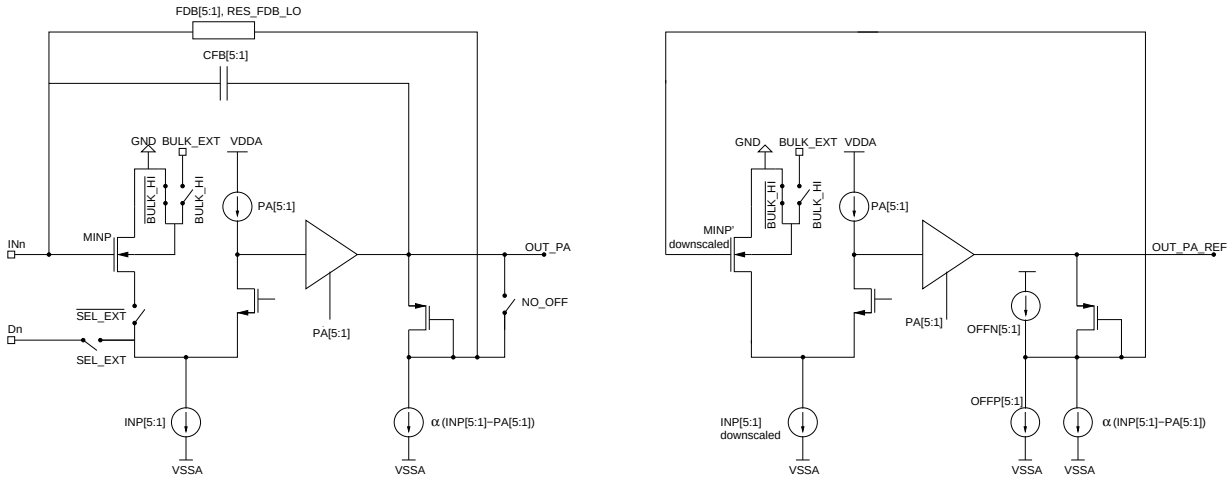


Figure 1: Preamplifier and reference preamplifier

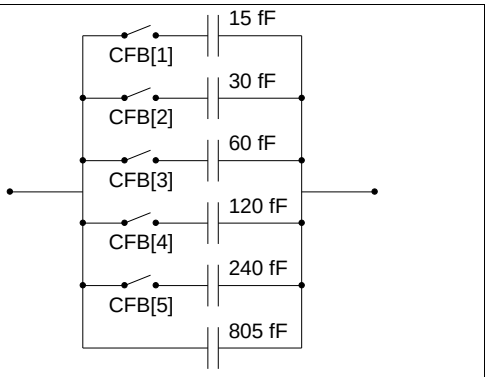


Figure 2: Adjustable feedback capacitor

Feedback Resistor

A feedback resistor sets the DC operation point of the integrating preamplifier preventing it from going into saturation by stacking pulses or by leakage current (Fig 3). For best noise performance, the feedback resistor should be as large as possible. For high pulse rates or leakage currents, the feedback resistance must be chosen lower.

A long NMOS operating in subthreshold region has been chosen for this purpose. Its value is controlled by register FDB[5:1] (fine adjust) as well as by range select bit RES_FDB_LO of the MODE[8:1] byte. The nominal resistance values are given in Table 3.

For positive charge pulses (which make the preamplifier output go low), both NMOS bulk and gate voltage have to follow the preamplifier output voltage to ensure a constant resistance value. This is due to the fact that NMOS operation is always refered to the most negative voltage applied at either drain or source. F-CSA104 can decide autonomously whether positive or negative charge pulses are input if AUTOSEL_N=0 (default). However, the charge polarity is fixed for a given detector system configuration, so that the user may specify the charge polarity channelwise using byte CHARGE_POS[8:1] (AUTOSEL_N=1).

It is recommended that the user makes use of the CHARGE_POS[8:1] byte in order to avoid any danger of switch noise by the Schmitt trigger otherwise operating.

Test Pulse

The test pulse generator allows for injecting charge pulses into the preamplifier inputs. All pulse generators share the common trigger input pad TP_TRIG_N so that all channels will simultaneously be affected. TP_TRIG_N leads to the input of inverters running between rails TP_LEV and GND. Adjustable capacitors couple the inverters' outputs to the preamplifier inputs. TP_LEV is a DC voltage supplied through an external pad used for setting the value of the test charge. TP_LEV may be connected to VDDA if a stable and clean VDDA is available or if the exact value of the test charge is not of concern.

For injecting a charge pulse, a 0->1 or 1->0 transition (TP_TRIG_N is an ordinary digital signal running between VDD and VSS) has to be applied to external pad TP_TRIG_N. TP_TRIG_N should normally be high to prevent noise from TP_LEV from coupling to the preamplifier input. The pulse capacitor is adjusted by CFB[5:3] i.e. by the same register controlling the feedback capacitor. Suitable values for TP_LEV can be taken from Table 4.

External p-channel FET

In cases where noise matching to higher capacitive detectors is required, or where flicker noise of the internal input PMOS proves to be insufficient, an external p-channel FET (Fig. 4) may be connected to F-CSA104. This feature might also allow for reuse of existing JFET-detector-systems (check that a

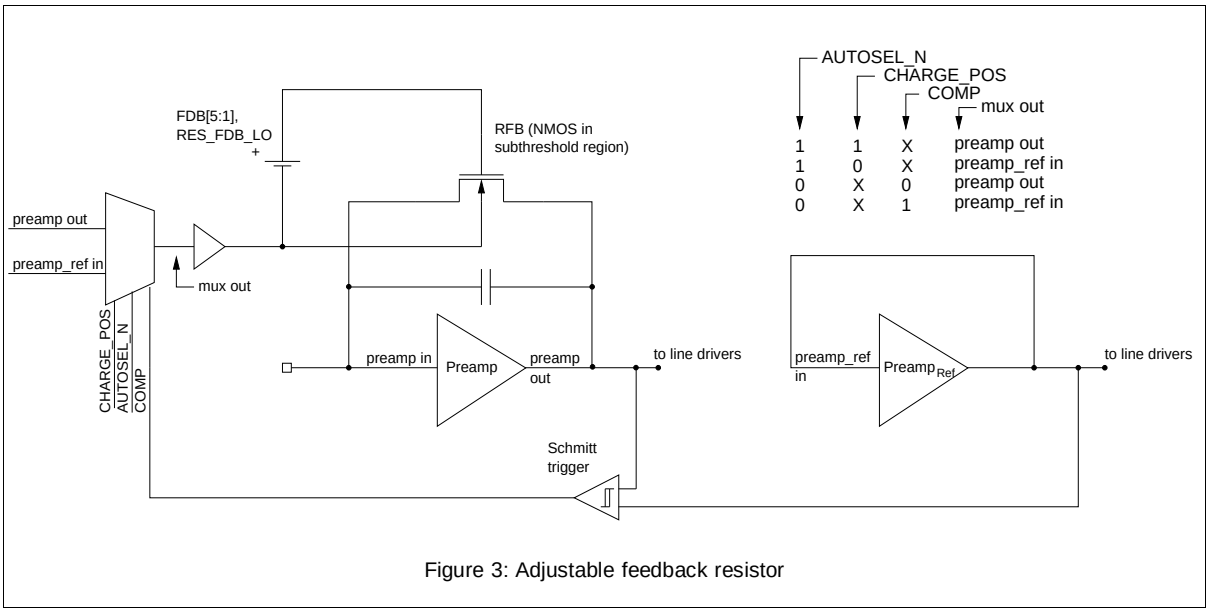


Figure 3: Adjustable feedback resistor

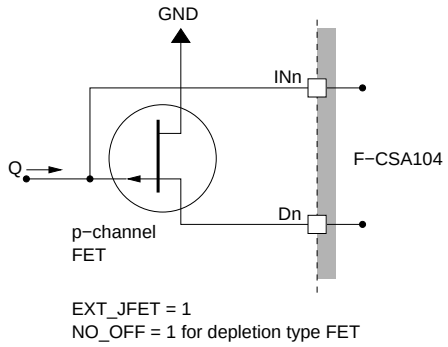


Figure 4: External p-channel FET

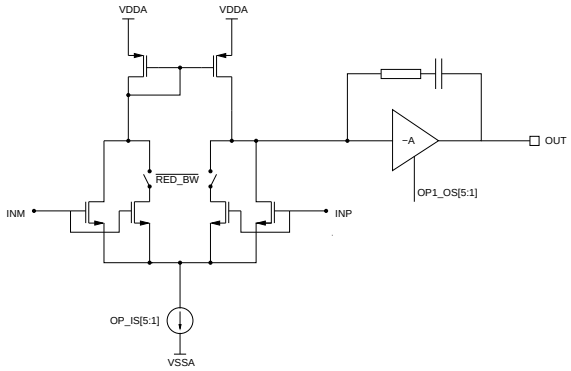


Figure 5: Line driver

p-channel JFET is used). Setting the SEL_EXT bit of MODE[8:1] byte shorts the internal PMOS and allows instead for the external FET's drain to couple its signal current to the preamplifier. The external FET's gate is connected to pad INn, its source and drain are to be connected to GND and pad Dn, respectively.

If a depletion device is used as exernal FET (e.g. a p-channel JFET), the NO_OFF bit of the MODE[8:1] byte should be set in order to short the preamplifier's level shifting MOS diode (Fig. 1).

Line Driver

Each channel of F-CSA104 features a differential output to minimize EMC (both actively and passively). Two fast, low offset operational amplifiers with high open loop gain and high current drive capability form the core of the drivers (Fig. 5). The operational amplifier used in the line drivers has particularly been designed for equal negative and positive rise/fall times. It is used in a differential amplifier configuration with fixed gain of three, subtracting preamplifier output voltage and reference preamplifier output voltage. The output voltages of positive and negative output channels are 0V in absence of a charge signal (for suppression of remaining offset voltages, see next section).

For operation at liquid nitrogen temperature, register setting OP1_IS[8:1] controling the bias current within the input stage of the operational amplifier should be lowered (Table 1) in order to keep the bandwidth of the line driver constant.

Offset supression

F-CSA104 does not employ AC coupling for offset supression. AC coupling is difficult to integrate on an IC due to the large time constant needed; also, it introduces the danger of baseline loss. Instead, F-CSA104 employs a triple DC offset suppression scheme.

First, offset given by the input transistor's threshold voltage is cancelled by an equal voltage drop over the MOS diode in the preamplifier's output section, being a scaled copy of the input transistor and operating at a likewise down-scaled operation current. Thus, the preamplifier output voltage would ideally be zero in the absence of any signal.

Secondly, any possibly remaining offset is cancelled by subtraction of preamplifier output and reference preamplifier output suffering from an equal offset.

Thirdly, registers OFFP[5:1] and OFFN [5:1] serve to manually adjust for any remaining offsets. Since these registers act on all channels of a chip, the channel offsets cannot be tuned individually.

An offset is introduced also by mismatch in the input differential stage of the operational amplifiers used as line drivers.

Any correlated offset of all operational amplifiers in the IC can be adjusted for by OFFP[5:1] and OFFN [5:1] in the same manner as for the preamplifier. Remaining individual offsets contribute to the output signals.

The individual channel offset voltages are expected to be fairly stable over dynamic range and should only slightly be dependent on temperature. If offsets need to be controlled even further, e.g. for highest precision spectroscopy tasks, it is recommended to use only one channel per chip, disabling the other channels using the PDOWN[8:1] register. The offset of the remaining channel can be tuned individually by registers OFFP[5:1] and OFFN [5:1].

I^2C Interface

An I^2C interface has been integrated for convenient adjustment of bias settings responding to particular application scenarios. F-CSA104 behaves as a standard mode I^2C-slave device supporting a transfer rate of 100 kbit/s. The I^2C-bus has been developed for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCLK). Note that SDA and SCLK signals are running between VDD and VSS, not GND. Weak pull up resistors to VDD of approx. 100 kΩ are integrated on the SDA and SCLK inputs for sustaining defined input voltages in the absence of external pull ups. The SCLK signal is always driven by the I^2C master, whereas the control over the SDA line changes between master and slave depending on read or write mode. Data transfer may be initiated by the master only when the bus is not busy.

More information about how to operate the I²C bus may be obtained from "The I²C-bus and how to use it", Philips Semiconductors, April 1995, available e.g. from www.philips.semiconductors.com.

The chip address is assigned to F-CSA104 via the address pads I2CADDR[7:1]. The address may be in the range from h'08 to h'77. The I2CADDR[7:1] pads contain pull down resistors; thus only ones have to be applied.

A register map of the F-CSA104's 15 internal registers controlling the amplifier settings along with the default values is given in Table 1. Fig. 6 explains the transfer sequences in write and read mode to access these 15 registers. Data is always transferred with the most significant bit (MSB) first. S, Sr, P, and A specify START condition, repeated START condition, STOP condition, and ACKNOWLDEGE bit, respectively.

In write mode, after having initialised the transfer by a START condition, the address of the chip ("slave") to be programmed is transmitted, followed by the register address and the data to be written to the target register. Every transmitted byte is acknowledged by F-CSA104.

The register address is auto-incremented by one after each transferred data byte according to the order given by Table 1. After the last byte transferred a STOP condition should be given. Data bytes in surplus of register 15 are ignored.

If all slave devices on the I²C bus should be programmed simultaneously, a general call can be used. A general call consists of (neglecting START, STOP and ACKNOWLDEGE) the general call address h'00, followed by the master device's address which identifies the master to the system. Next follow register address and data byte(s).

For a read back of F-CSA104's registers, the I²C bus needs to be initialised, followed by the chip address and the register address. The I²C-bus is re-initialised by a repeated START condition, the chip address is sent and data is read out. If multiple bytes are read out, the register address is auto-incremented. The read sequence should be terminated by a STOP condition.

Setting the register address and reading of register data may be separated into two distinct commands. To do so, the repeated START condition (Sr) in Fig. 6 is to be replaced by a STOP (P) and a START (S) condition.

Figure 6: I²C Data transfer

Noise performance

F-CSA104 has been optimized for detectors of 0 - 100pF. The noise performance of F-CSA104 for different detector capacitances and shaper times (CR-(RC)^4 shaping) at room temperature (for other settings see ENC_{RT} in section "Electrical Characteristics") has been plotted in Figs. 7 and 8.

Application

F-CSA104 can be DC- or AC-connected to a semiconductor detector. When DC-coupled (Fig. 9), the virtual ground potential delivered by the preamplifier input (-1.1V) is being applied to the detector's signal electrode, causing an electrical field in the detector when HV (high voltage, either positive or negative) is applied to the detectors's counter electrode. With DC-coupling, detector leakage currents may enter the preamplifier and may cause it to saturate. Using AC-coupling (Fig. 10), there is no danger of leakage currents saturating the preamplifier, but charge is lost depending on the ratio of couple capacitor to detector capacitor. Also, an extra resistor for biasing the detector's signal electrode is required which causes extra thermal and flicker noise. Depending on signal rate, noise requirements, and the couple method chosen, the preamplifier's feedback resistor can be adjusted using settings RES_FDB_LO and FDB[5:1]. The

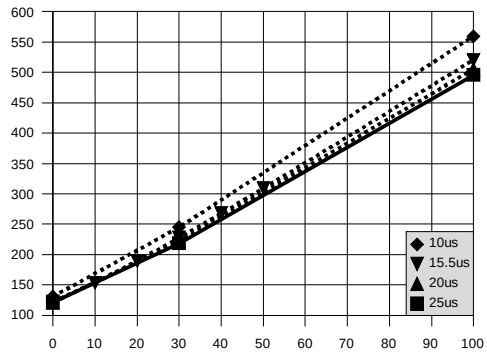


Figure 7: ENC vs C_{det} (0 .. 100pF)

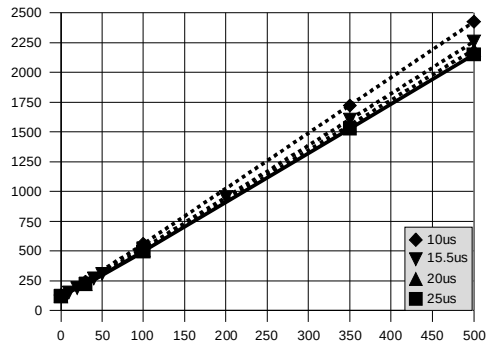


Figure 8: ENC vs C_{det} (0 .. 500pF)

lower the value of the feedback resistor is chosen, the more robust the preamplifier works, but also the higher the noise contribution by the feedback resistor is.

The preamplifier refers any input signal directly to GND (the virtual ground potential of the preamplifier's input follows GND). It is therefore of greatest importance that the GND potential applied to F-CSA104 is free from any interference and is very well connected to the ground potential used by the detector's HV supply (and the ground potential used with the bias resistor when AC-coupling). Any voltage difference ΔV between the detector ground and F-CSA104's GND will cause a charge injection of $\Delta V \cdot C_{det}$! It is therefore recommended to route GND separately to F-CSA104 and not to use it for capacitive filtering of VDDA and VSSA.

Care should also be taken for quiet power supplies VDDA and VSSA. VDDA and VSSA should be filtered with filter capacitors to GND potential each, using a separate connection to the GND star-point (Figs. 9 and 10).

F-CSA104's differential output lines should be connected to a receiver as shown in Fig. 11. 50 Ω resistors ensure impedance matching to the 100 Ω twisted pair transmission cable. A particularly low-ohmic ground connection between F-CSA104 and the receiver is not required due to the differential nature of the signal connection. If no signal transmission to a distant receiver is required, an ADC with (differential) input impedance of 200 Ω or more may be directly attached to F-CSA104's output.

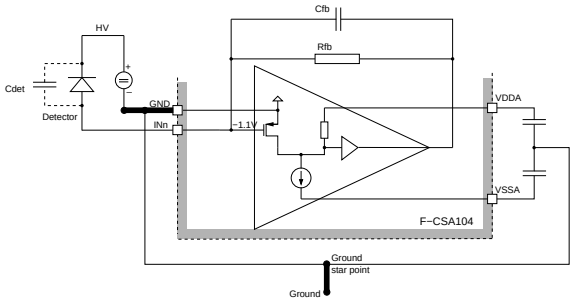


Figure 9: F-CSA104 DC-coupled to detector

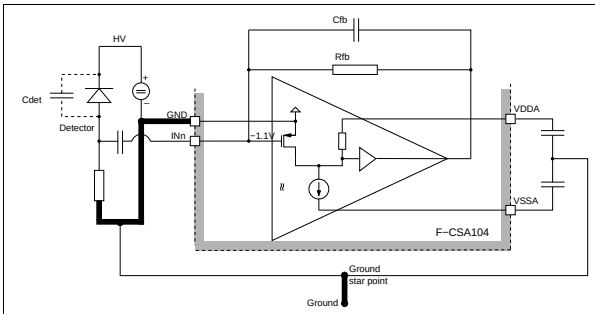


Figure 10: F-CSA104 AC-coupled to detector

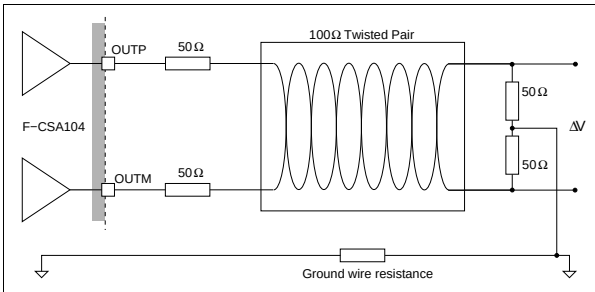


Figure 11: Connection to signal receiver

Tables

Unless otherwise specified, all values given are for T=27°C, register settings „default 27°C“, VDDA=VDDD =-VSSA=-VSSS = 2.5V, GND=0V, R_{load} = 100 Ω.

A	Name		Description	Default 27°C	Def. -200°C
1	PDOWN[8:1]		Power down bit mask (bit 1 -> channel 1, bit 2 -> channel 2, ...)	h'00	h'00
2	CFB[8:1]		Preamplifier feedback capacitor adjustment (see Formula 1)	h'0D	h'0D
3	TESTSEL[8:1]		Test control register	h'00	h'00
4	MODE[8]	EXT_JFET	Connect p-FET externally	0	0
	MODE[7]	BULK_HI	Connect input transistor bulk to BULK_EXT (instead of GND)	0	0
	MODE[6]	AUTOSEL_N	Autoselect of charge polarity	0	0
	MODE[5]	NO_OFF	Shorts MOS level shifting diode in preamplifier	0	0
	MODE[4]	RED_BW	Reduces bandwidth of line driver	0	0
	MODE[3]	TEST_N	Test mode	1	1
	MODE[2]	RES_FDB_LO	Preamplifier resistive feedback values in low range (see Table 3)	1	1
	MODE[1]	RES	reserved	0	0
5	FDB[8:1]		Preamplifier resistive feedback adjust (see Table 3)	H'05	h'05
6	BUF[8:1]		Bias current of Schmitt trigger and Rail-to-rail amplifier	h'08	h'08
7	PA[8:1]		Preamplifier bias current	h'08	h'08
8	INP[8:1]		Input transistor current	h'08	h'08
9	OP1_IS[8:1]		Line driver input stage current	h'08	h'06
A	OP1_OS[8:1]		Line driver output stage current	h'08	h'08
B	RESERVED		Always set to h'00	h'00	h'00
C	RESERVED		Always set to h'00	h'00	h'00
D	OFFP[8:1]		Offset adjust (V(OUTP-OUTM) increases, see Table 2)	h'00	h'00
E	OFFN[8:1]		Offset adjust (V(OUTP-OUTM) decreases, see Table 2)	h'00	h'00
F	CHARGE_POS[8:1]		Bit mask for charge polarities (bit 1 -> channel 1, bit 2 -> channel 2, ...)	h'00	h'00

At power up, the 27°C default settings are loaded. Values marked in red differ for 27°C and -200°C.

Table 1: Control register map with address and default values

OFFP[5:1]	ΔV(OUTP-OUTM) [mV]	OFFN[5:1]	ΔV(OUTP-OUTM) [mV]
h'00	0	h'00	0
h'01	+8.6	h'01	-3.6
h'02	+16.7	h'02	-8.0
h'03	+23.9	h'03	-12.0
h'08	+59.0	h'08	-34.9
h'10	+108.7	h'10	-74.0
h'18	+152.5	h'18	-118.5
h'1F	+186.6	h'1F	-163.6

Table 2: Offset tuning steps with OFFP[5:1] and OFFN[5:1]

$$C_{FB} = 805fF + CFB[5]\cdot 240fF + CFB[4]\cdot 120fF + CFB[3]\cdot 60fF + CFB[2]\cdot 30fF + CFB[1]\cdot 15fF$$

Formula 1: Feedback capacitor value; C_{FB} = 1pF for CFB[5:1] = h'0D

RES_FDB_LO	FDB[5:1]	Resistance [Ω]	RES_FDB_LO	FDB[5:1]	Resistance [Ω]
0	h'01	2.211E+09	1	h'01	8.152E+06
	h'02	1.080E+09		h'02	5.052E+06
	h'03	7.159E+08		h'03	3.882E+06
	h'04	5.359E+08		h'04	3.241E+06
	h'05	4.286E+08		h'05	2.827E+05
	h'06	3.573E+08		h'06	2.534E+06
	h'07	3.061E+08		h'07	2.312E+06
	h'08	2.686E+08		h'08	2.137E+06
	h'09	2.391E+08		h'09	1.996E+06
	h'0A	2.155E+08		h'0A	1.878E+06
	h'10	1.362E+08		h'10	1.438E+06
	h'18	9.231E+07		h'18	1.149E+06
	h'1F	7.257E+07		h'1F	1.000E+06

Table 3: Selectable feedback resistor values

TP_LEVEL [mV]	Charge [fC]	Energy [MeV (Ge)*]	Energy [MeV (Si)*]
1015	100	1.850	2.263
2030	200	3.700	4.525
2500	246	4.551	5.566
549	54.1	1	1.223
449	44.2	0.818	1

*: Germanium: 2.96 eV/electron-hole-pair (T=-196°C), Silicon: 3.62 eV/electron-hole-pair (T=27°C)

Table 4: Testpulse charges for different TP_LEV voltages for calibrated C_{pulse} = 98.5 fF

Name	I/O	Analog/digital	Description
IN[1]-IN[4]	Input	Analog	Amplifier inputs
OUTP[1]-OUTP[4]	Output	Analog	Positive polarity amplifier output
OUTM[1]-OUTM[4]	Output	Analog	Negative polarity amplifier output
TP_TRIG_N	Input	Digital	Active low test pulse trigger
TP_LEVEL	Input	Analog	DC voltage defining test pulse charge
BULK_EXT	Input	Analog	External bulk connection terminal
SCL	Input	Digital	I^2C clock
SDATA	Input/ouput	Digital	I^2C data
I2CADDR[7:1]	Input	Digital	I^2C address
RESET_B	Input	Digital	Active low reset
VDDA	Input	Power	Positive analog power supply (+2.5V)
VSSA	Input	Power	Negative analog power supply (-2.5V)
GND	Input	Ground	Analog ground (0V)

Table 5: F-CSA104 I/O Pads

Electrical Characteristics

Unless otherwise specified, all values given are for T=27°C,register settings „default 27°C“, VDDA=VDDD =-VSSA=-VSSS = 2.5V, GND=0V, R_{load} = 100 Ω; **all values at -200°C have been derived from simulations with estimated models.**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ENC_{RT}	Input equivalent noise charge at room temperature	CR-$(RC)^4$ shaper, peak time 20µs, AUTOSEL_N=1, RES_FDB_LO=0 C_{det} = 0 pF C_{det} = 30 pF C_{det} = 100 pF		 120 220 510		 electrons electrons electrons
$FWHM(Si)_{RT}$	“Electronic noise” contribution when used with silicon detector at room temperature	CR-$(RC)^4$ shaper, peak time 20µs, AUTOSEL_N=1, RES_FDB_LO=0 C_{det} = 0 pF C_{det} = 30 pF C_{det} = 100 pF		 1.02 1.87 4.24		 keV keV keV
ENC_{LT}	Input equivalent noise charge at -200°C	CR-$(RC)^4$ shaper, peak time 20µs, AUTOSEL_N=1, RES_FDB_LO=0, remaining settings “default -200°C” C_{det} = 0 pF C_{det} = 30 pF C_{det} = 100 pF		 60 110 240		 electrons electrons electrons
$FWHM(Ge)_{LT}$	“Electronic noise” contribution when used with Germanium detector at -200°C	CR-$(RC)^4$ shaper, peak time 20µs, AUTOSEL_N=1, RES_FDB_LO=0 C_{det} = 0 pF C_{det} = 30 pF C_{det} = 100 pF		 0.417 0.765 1.67		 keV keV keV
$g_{m,RT}$	Input transistor transconductance	I_{inp}=1mA (INP=h'08), T=27°C		19.7		mA/V
$g_{m,LT}$	Input transistor transconductance	I_{inp}=1mA (INP=h'08), T=-200°C		39.2		mA/V
C_{gate}	Input capacitance	Input capacitance of input PMOS (W=9000µm, L=0.6µm)		7		pF
A_V	Charge sensitivity V(OUTP-OUTM) / Q_{in}	AUTOSEL_N=1, RES_FDB_LO=0, remaining settings “default -200°C”, Positive input charge Q_{in} > 0 Negative input charge Q_{in} < 0		 5.84 315.7 258.1 5.84 315.7 258.1		 mV/fC mV/MeV(Ge) mV/MeV(Si) mV/fC mV/MeV(Ge) mV/MeV(Si)
V_{pp}	Dynamic range	AUTOSEL_N=1, RES_FDB_LO=0, remaining settings “default -200°C”, Positive input charge Q_{in} > 0 Positive input charge Q_{in} > 0		 600 11.1 13.6 600 11.1 13.6		 fC MeV(Ge) MeV(Si) fC MeV(Ge) MeV(Si)
INL	Integral nonlinearity	AUTOSEL_N=1, RES_FDB_LO=0, remaining settings “default -200°C”, measured after 1µs, LSB (14 bit) refered to dynamic range V_{pp} Positive input charge Q_{in} > 0 Negative input charge Q_{in} < 0		 2 1		 LSB LSB
XT	Interchannel crosstalk				1	‰
T_r	Risetime 10%-90%	Q_{in} = 40 fC Q_{in} = 541 fC (= 10 MeV(Ge))		22 28		ns ns

T_s	Settling time for 14 bit accuracy	Q_{in} = 40 fC, ΔV(OUTP-OUTM)=14 µV Q_{in} = 541 fC, ΔV(OUTP-OUTM)=190 µV		560 530	700 700	ns ns
$T_{1/2}$	Preamplifier decay time (half life) for small Q_{in}	Minimum value: RES_FDB_LO = 1, FDB[5:1] = h'1F maximum value: RES_FDB_LO = 0, FDB[5:1] = h'01	0.7		1530	µs
$A_{o,PA}$	Preamplifier open loop gain			120		dB
$A_{o,OP1}$	Line driver open loop gain			92		dB
ΔV_{in}	Input voltage shift for max positive/negative signal after settling			0.44		µV
I_{DD}	Current consumption	No traffic on I^2C lines, no signal injected			60	mA
$I_{DD,CH}$	Current consumption per channel (VSSA)	No signal injected			9.5	mA
V_{off}	Offset voltage					
$V_{off,D}$	Offset voltage shift over dynamic range					
$V_{off,T}$	Offset voltage shift with temperature					

Maximum Ratings

Maximum supply voltage for lifetime of 10 years:	5.25V
Maximum input charge for lifetime of 10 years:	600fC
Absolute maximum supply voltage (exposure may affect functionality and lifetime):	6.65V

F-CSA104 has been jointly developed by Max-Planck-Institute für Kernphysik, Heidelberg and FBE ASIC Design & Consulting. Please direct enquiries regarding academical use of F-CSA104 to MPI für Kernphysik. For commercial applications of F-CSA104, please direct your questions to FBE ASIC Design & Consulting.

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