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Design of the MTC 6210
10Gbit NextGeneration SDH/SONET framer

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Overview

- Motivation
- From idea to a system – the VC-core of the Multilink 10Gbit SDH/SONET-Framer
  - Project history
  - System description
- Conclusion
  - Why use a graphical system ??
  - Cons of using VisualElite
- About me

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Motivation

- Digital design is system design
  - Designflow should be always a TopDown-Flow
  - Specification for subblocks should be executable
  - Specification ALWAYS change during design
- So, the ideal design-environment has to:
  - Allow a design on the highest possible abstraction-level
  - Support a selfdocumented design (written specs and documentation don't keep pace of design)
  - Be easy maintainable (interface to version control)
  - Allow different types of design-representation (behav. models, RTL, dummy-models, SystemC,...)
  - Simple interface to other EDA-tools (synthesis, simulation, ...)

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From idea to a system – Design of a 10Gbit-Framer

Business-Situation at project-start in 08/2000:

- Multilink wants to expand from its physical layer postion into new markets esp. into VLSI-chipsets for SDH/SONET but has no real expertise in framer-design ==> Collaboration with IBM on framer-design
  - 1st task : Verification of an IBM 10Gbit framer with ATM-interface, stopped in 10/2000 because late to market (according to marketing)
  - 2nd task : Joint development of a 40Gbit-framer
- After the 10Gbit framer stop, start of the predevelopment for a 10Gbit NextGen-framer with a workshop together with IBM system engineers
  - Result is a 1st level spec on paper with some ideas
  - IBM focuses later on 40Gbit and MLTC has not enough ressources to staff the project

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Project-Setup

- Project is started as an „IP“-development with the „paper“-spec to gain system-expertise with 3 (later 4) engineers
- Standardization for NextGeneration SDH/SONET-equipment still ongoing
- Using Summit-Visual, 3 month later the interfaces and the major subblocks are specified (and partly simulatable) for the features written in the original spec (VC, LCAS, 2ms pathdelay in internal DRAM)
- 02/2001 MLTC decides to start product-design on 3 sites (40..60 engineers)with planned tape-out in end of 2001
- 05/2001 Complete redefinition of the VC-core after more marketing-input ==> internal memory now for only 2 frames(0.33ms) / external DDR-SDRAM for up to 128 multiframes (256ms)

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Key numbers:

- Technology : IBM-0.13 um
- Gate-Count (non-memory) : appx. 4.5M
- Memory (frame-memory and packet-memory only) : ca 700 kByte
- IO-bandwidth :
  - Line-IF 16bit /622 Mhz
  - Packet-IF SPI-4 / 16bit /up to 800 Mhz / 64 payload-channel
  - DDR-SDRAM-IF 128bit /155...180 MHz
- Core-bandwidth : 72/64bit / 155 Mhz

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Design environment

- Design-HDL : VHDL
- Design-environment : Summit-VisualHDL for VC-core, others in plain VHDL, SDRAM-controller in Verilog
- Version control: Synchronicity with central DB in Somerset(US) and mirrors on design-sites
- Verification-environment : Specman/Modelsim/Quickturn
- Synthesis/STA : Synopsys-DC / Primetime
- DesignForTestability : IBM
- Backend : IBM

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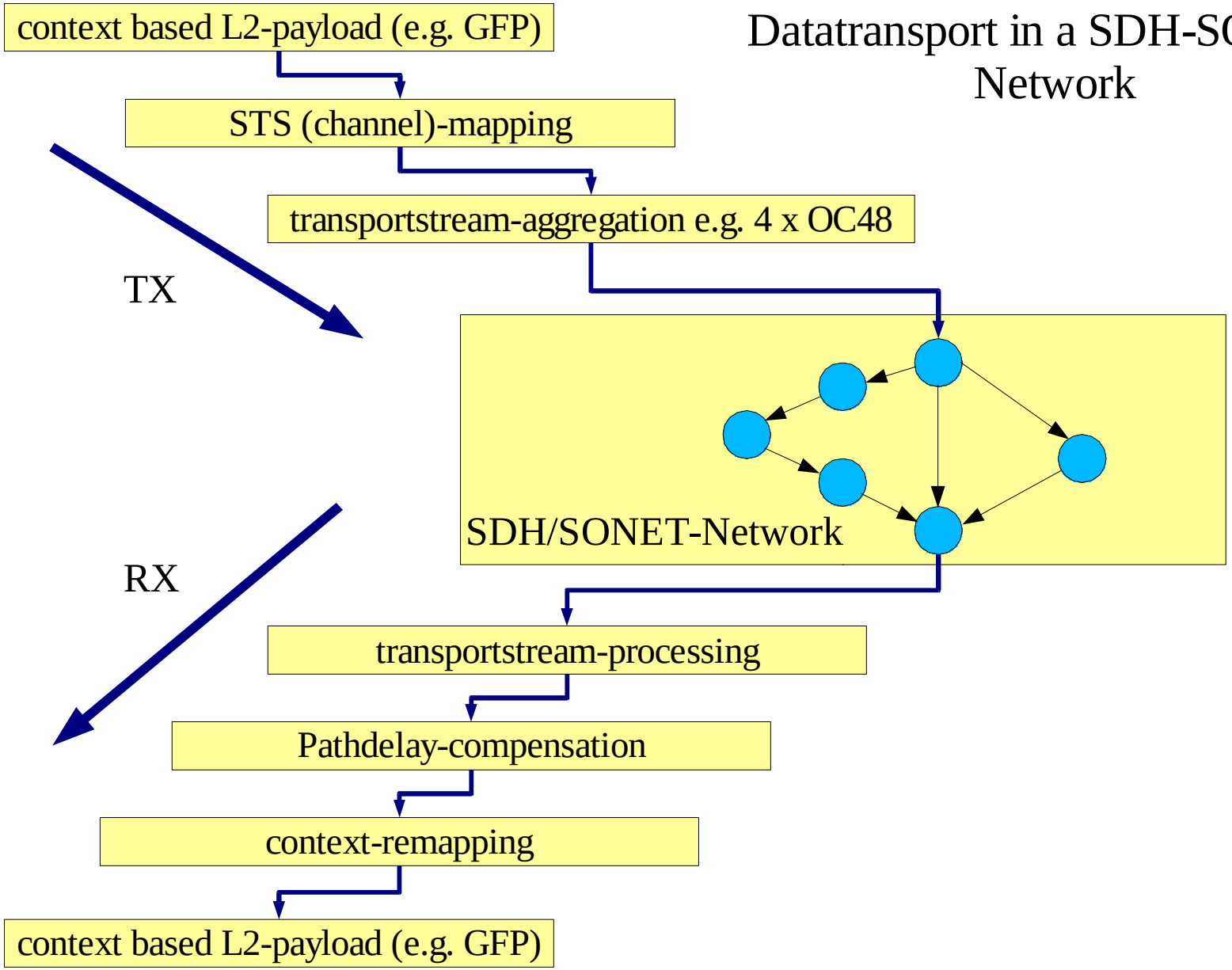

Datatransport in a SDH-SONET-Network

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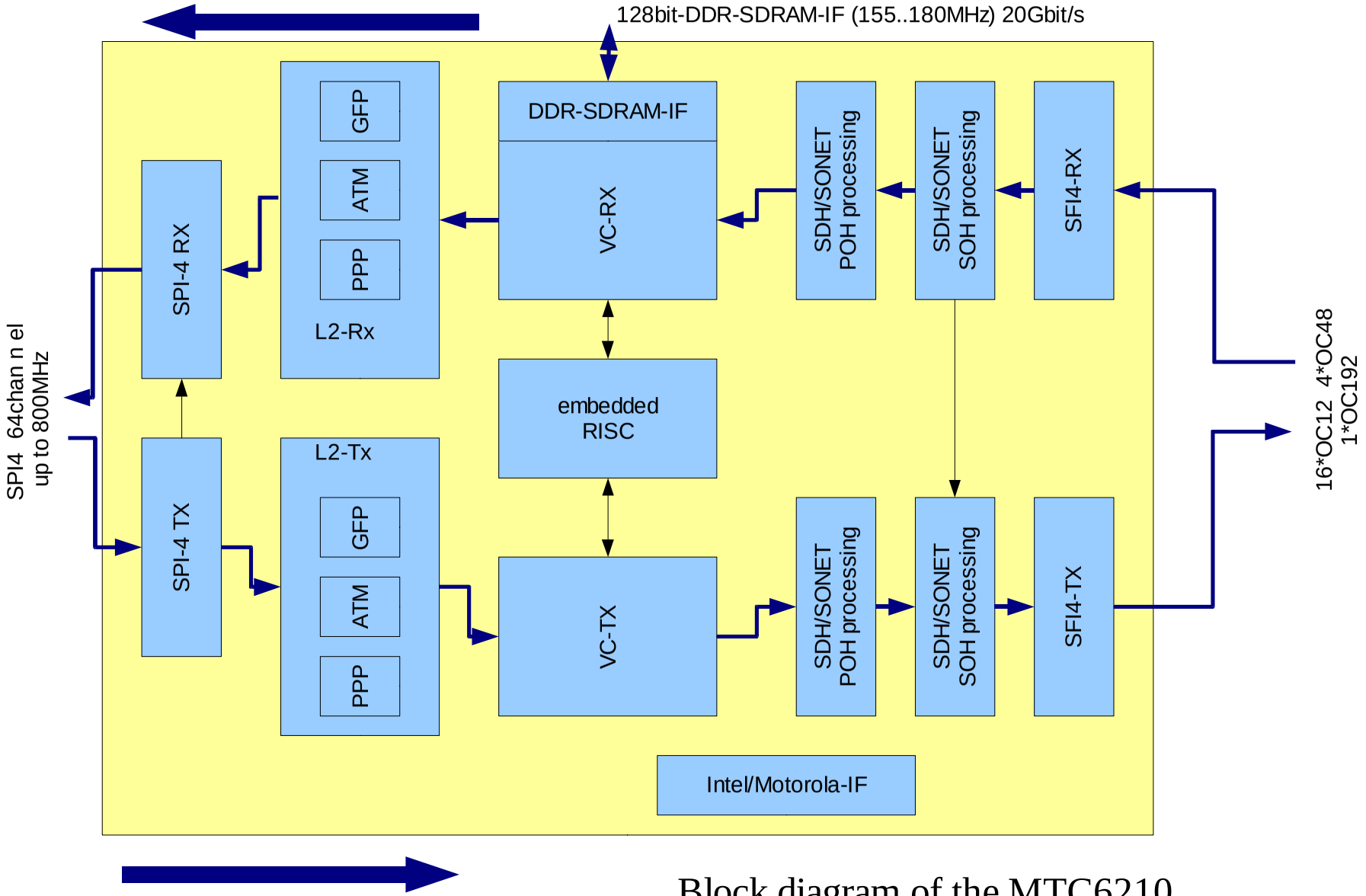

Block diagram of the MTC6210

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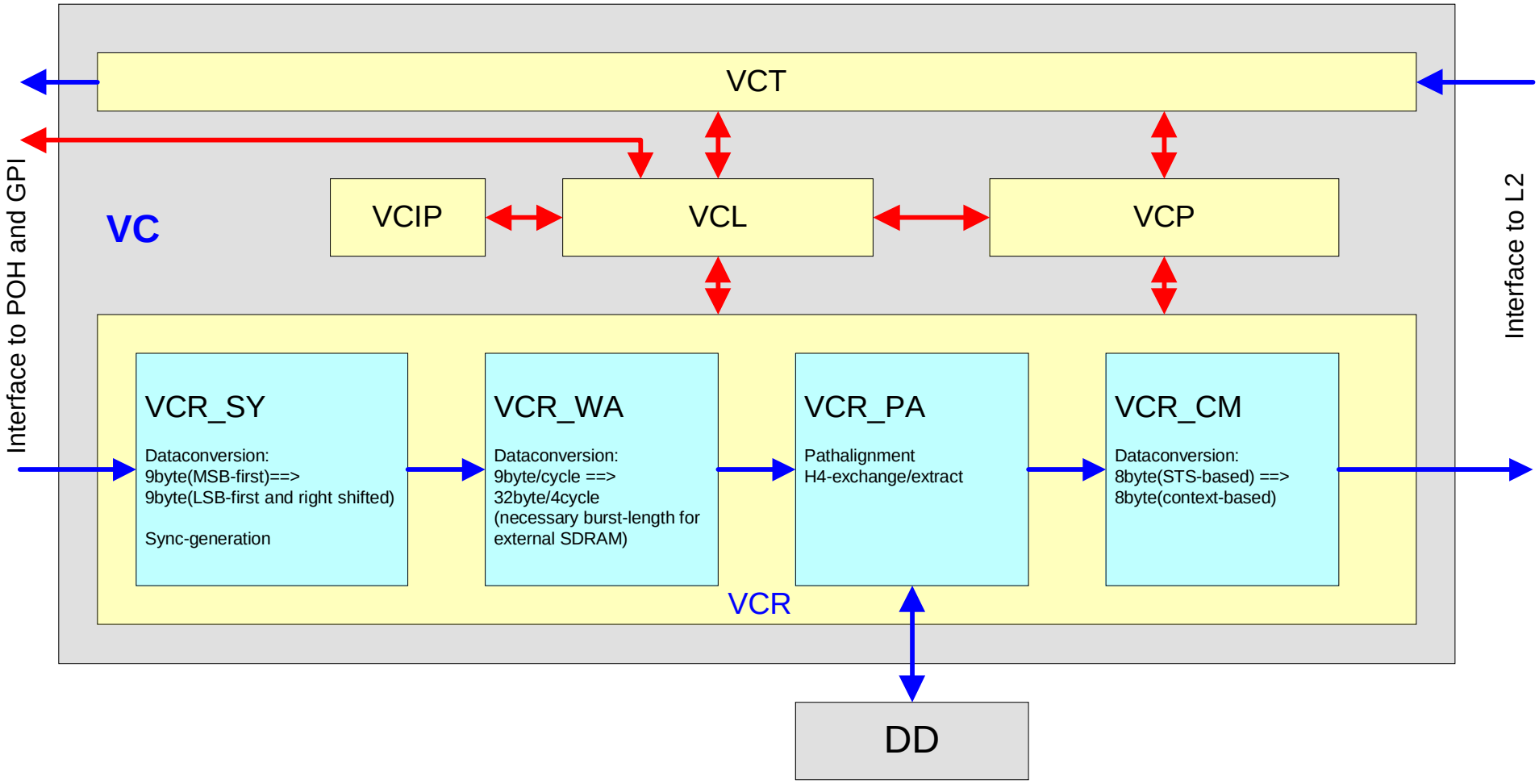
Block diagram of the VC-core



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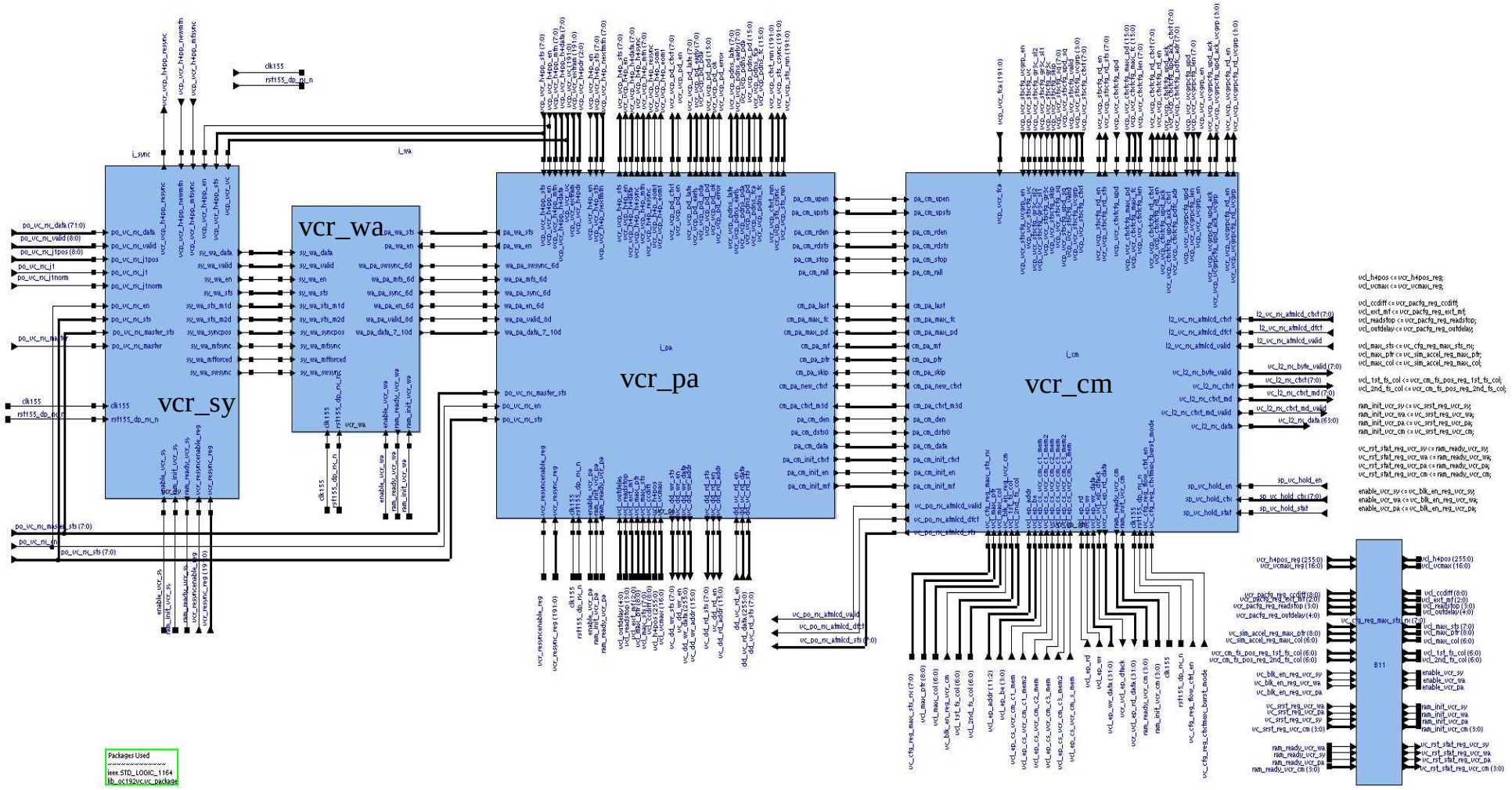
Block diagram of the VC-RX-core



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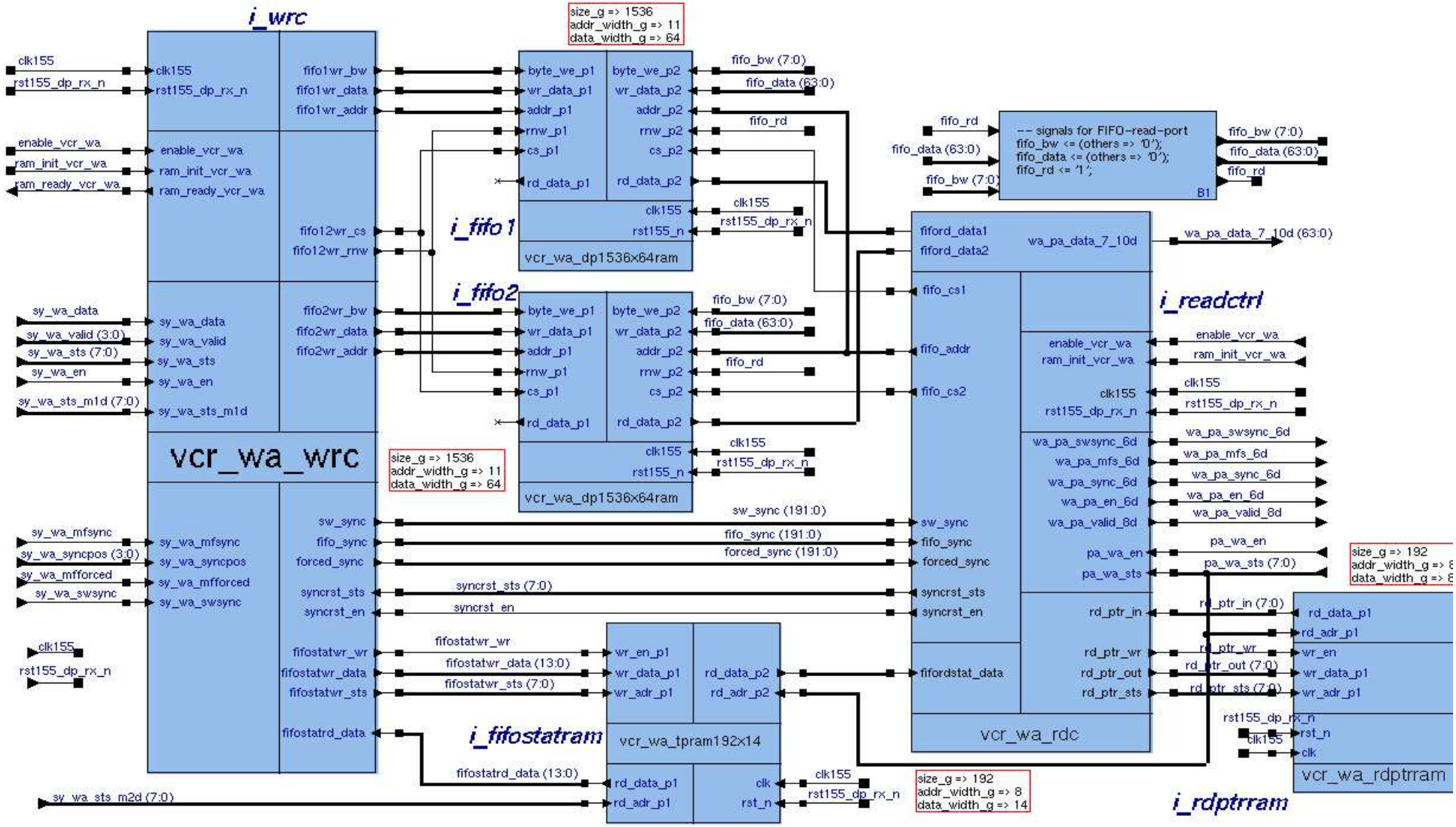
Block-diagram of the VCR-Wordalignment



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Conclusion : Why use a graphical system ??

- Much better selfdocumentation of the code
- Better maintanable because of the much better overview
- Easier to put the design together
- Integrated interface to version-control
- For beginners it's much easier to do the 1st steps in ASIC-designs
- It can visualize dependencies much better than plain code
- It's more fun to work with a graphic tool than with even the best text-editor

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Cons of using VisualElite

- You have to pay for the license (just a joke, but normally the only reason, not to use the tool)
- Only 1 architecture per entity w/o library-change
- Only 1 export-directory (OK only, when database contains Summit-data and not HDL-code)
- Unnamed unit-directories (p1/...) are a pain if you have to modify the database (e.g. for renaming)
- Important features of VersionControl like Release-upload,... are not (or not well) supported.
- It would be fine to have a documentation-link for each design-unit.

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Who I am

- Graduated in 1998 at TU-Berlin with the design of a neural connection processor
- 1998 - 1999 HHI-Berlin - working at a MPEG-II-decoder and a HDTV-video-format-converter
- 1999 - 2000 Rohde&Schwarz - responsible for memory-subsystem and processor-interfaces of a chipset (ASICs + FPGA) for digital signal processing
- 2000 - 2002 Multilink Techn. - Lead Designer for 10Gbit-SDH/SONET-framer (responsible for VC-Rx and SPI4-interface as well as project manager for verification environment)
- 2002 - 2003 SonyEricsson – Systemarchitect and project manager for the design of a mobile 3D-coprocessor
- 2003 - ... Infineon Technologies working on the digital part of a 2Gbit-Flash-RAM