FBE-ASIC GmbH

Meet quality, cost and schedule in verification

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Automated verification environments for SOC families

Ludwigshafen • Berlin

Index

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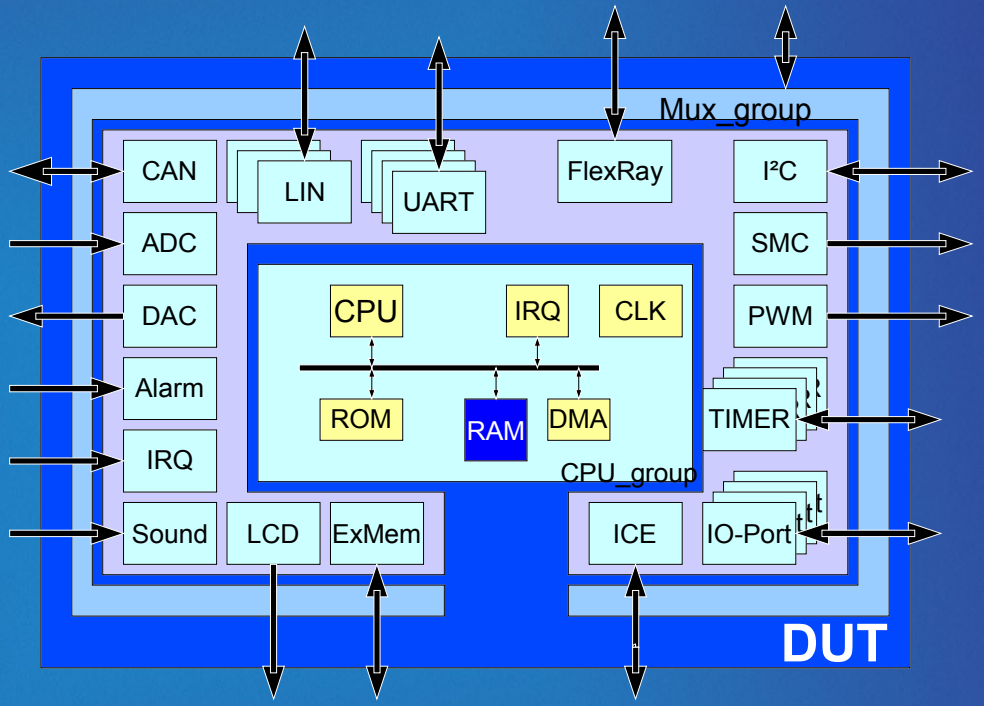
- Introduction – Motivation
- SOC – families today
- What is normally verified ?
- What needs to be verified ?
- How long does it need to get the device verified ?
- Can it be automated ?
- What needs to be considered ?
- The end

- More than 50 % of complex ICs need at least one redesign caused by functional errors.
- Verification closure is often not predictable.
- Verification time consumes already more than 50% of the design time
- Technology and design keeping pace with Moore's Law (doubling the possible complexity within 2 years) – Verification still falls behind.
- Verification (and also system engineering) doesn't scale linearly but exponentially

SOC – families today

Example Microcontroller

- Infineon - 8bit > 25 devices
- Infineon - 16bit >120 devices
- Infineon - 32bit >16 devices
- Atmel - 8bit >50 devices
- Atmel - 32bit >15 devices
- Freescale - 8bit >30 devices
- Freescale - 32bit >50 devices

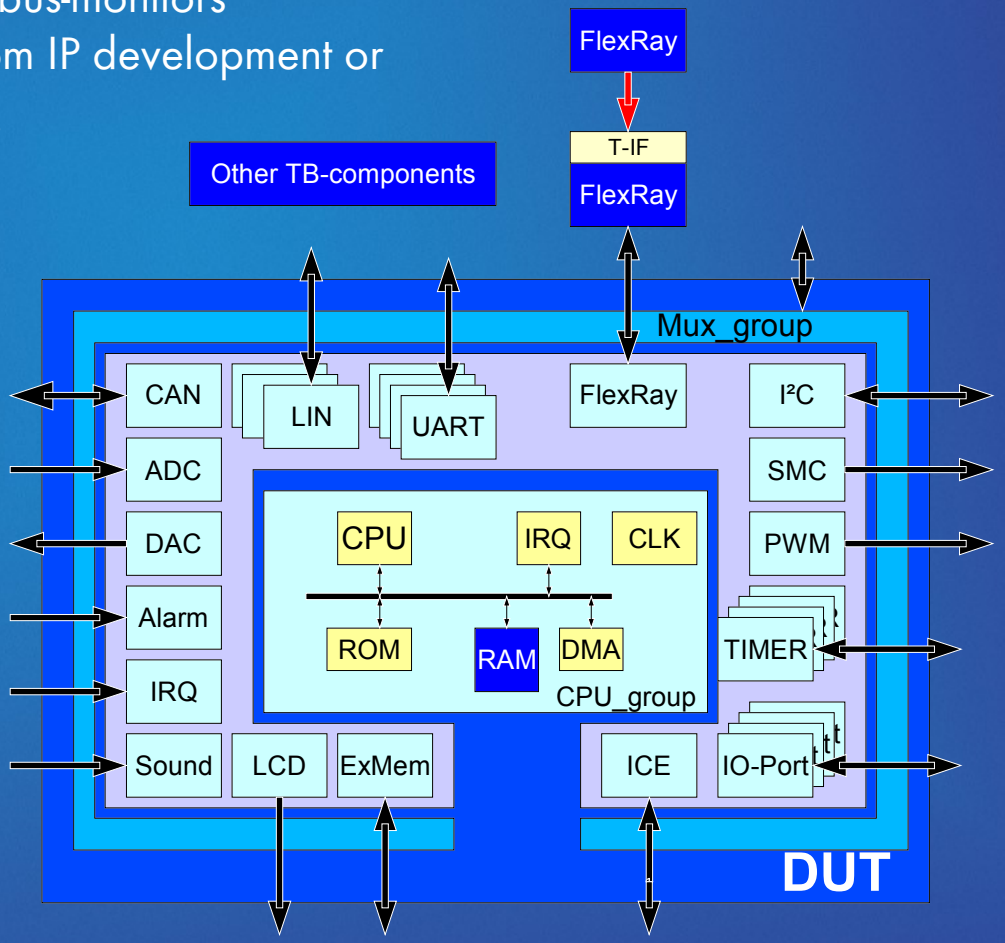


What are the main differentiators between these devices ?

- The processor-kernel – rarely
- Memories – sometimes
- Peripherals – always
- I/O-Pads - always

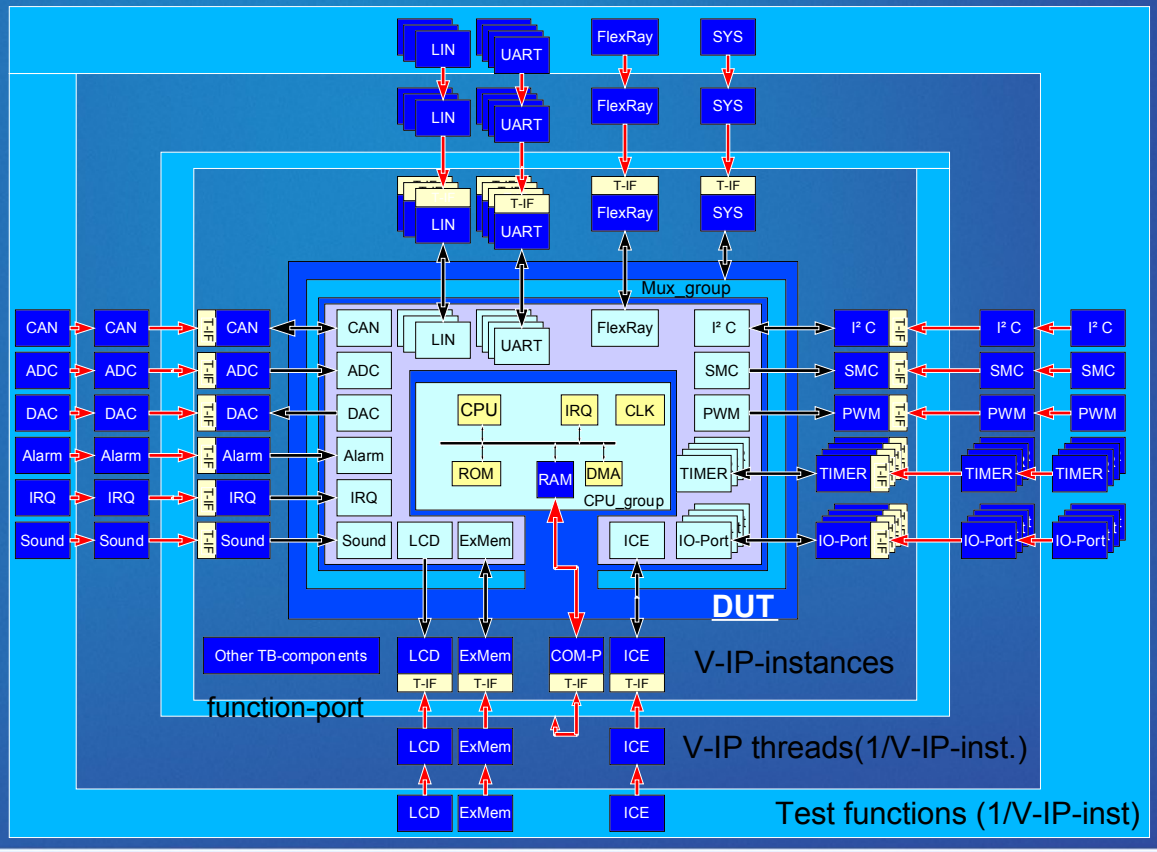
What is normally verified ?

- Processor-kernel using functional pattern from processor-development or using integration tests
- Bussystems using integration tests and bus-monitors
- Peripherals using functional pattern from IP development or so called integration tests for single IPs



What needs to be verified ?

- The performance of the complete system (response times etc.)
- Connectivity between processor kernel and peripherals
- Connectivity between peripherals and I/O-MUX
- Connectivity between I/O-MUX and I/Os
- The I/O-MUX



How long does it need to get the device verified ?

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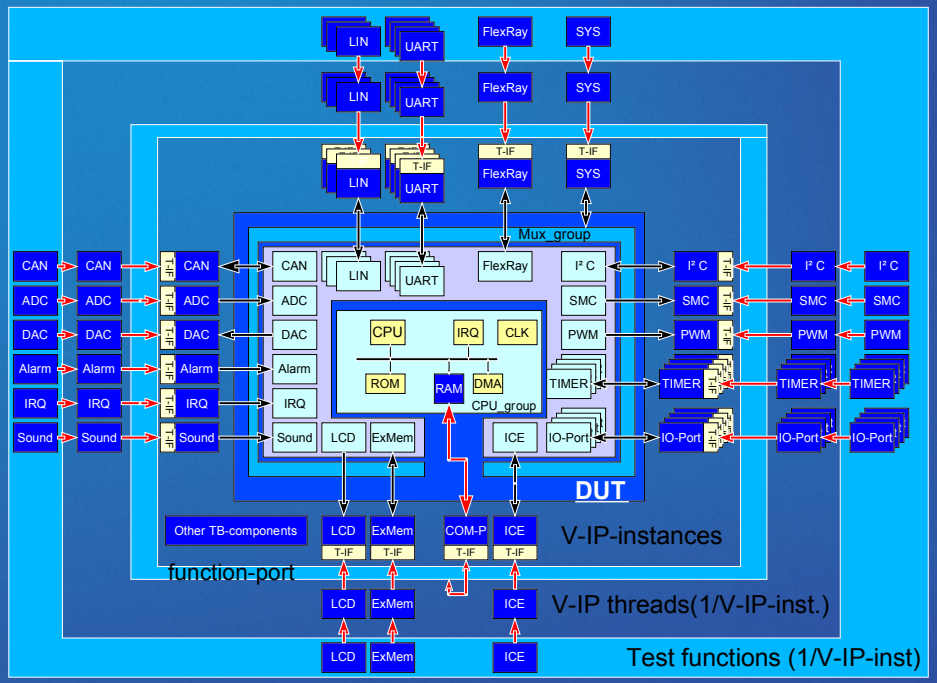
- Testplan generation
- Testbench generation
- Test generation
- Simulation / Emulation runtime
- Test + Coverage postprocessing



How long does it need to get the device verified ?

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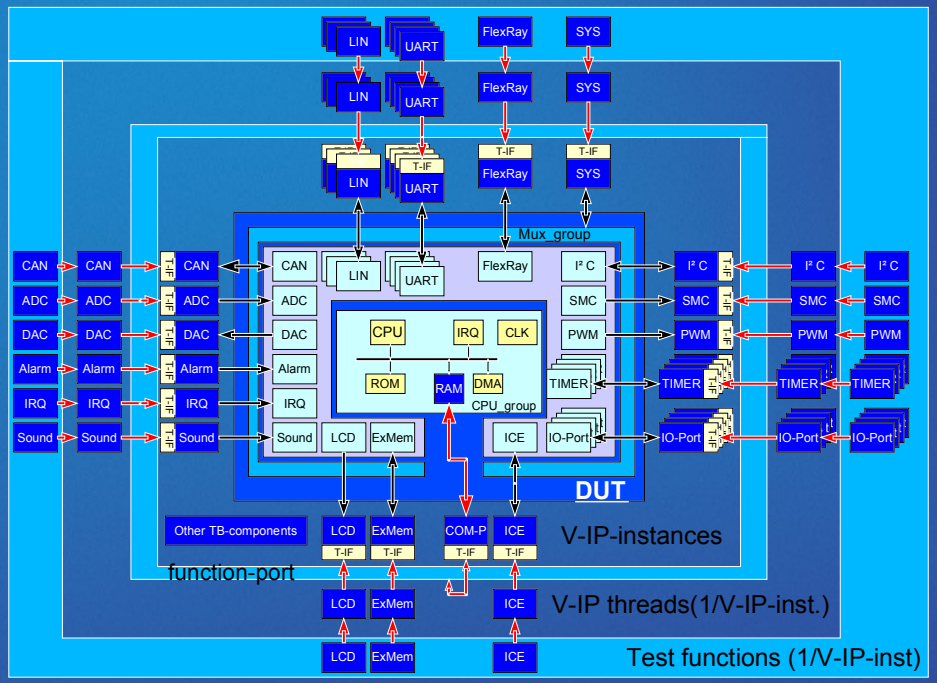
• Testplan generation	>> 2 weeks
• Testbench generation	>> 1 .. 12 month
• Test generation	>> 1 .. 4 month
• Simulation / Emulation runtime	>> 1 week .. 1 month .. XX years
• Test + Coverage postprocessing	>> 1 week
SUM	3 month .. XX years



Can it be automated ?

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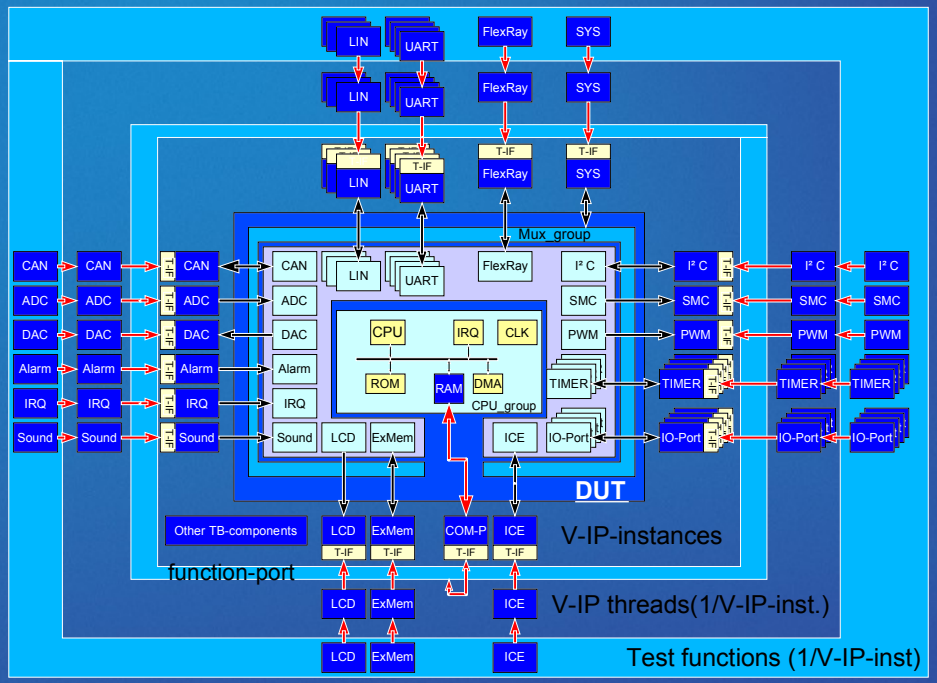
- Testplan generation >> difficult
- Testbench generation >> yes
- Test generation >> yes
- Simulation / Emulation runtime >> yes, but no big gain
- Test + Coverage postprocessing >> yes



Can it be automated ? - What are the benefits ?

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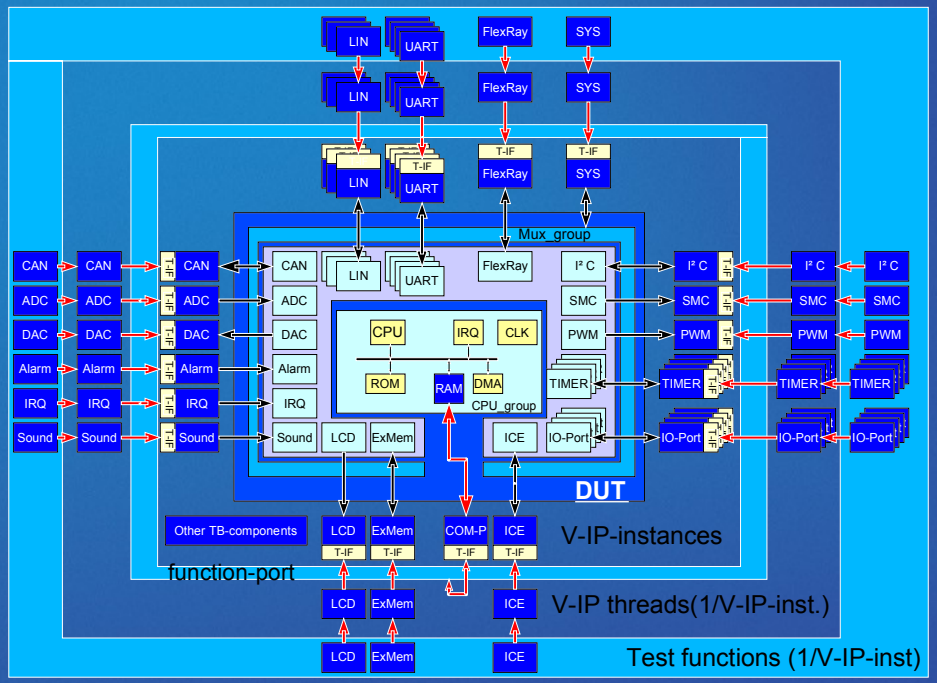
• Testplan generation	>> difficult	>> 0 days
• Testbench generation	>> yes	>> ½ day
• Test generation	>> yes	>> ½ day
• Simulation / Emulation runtime	>> yes, but no big gain	>> 1 week ... some years
• Test + Coverage postprocessing	>> yes	>> ½ day
SUM		**2 weeks .. XX years**

Other benefits for derivatives

- No errors from testbench and test development
- Meets schedule and cost targets
- Integrates into new SOC design automation methodes based on SPIRIT standardization



What needs to be considered on management side ?

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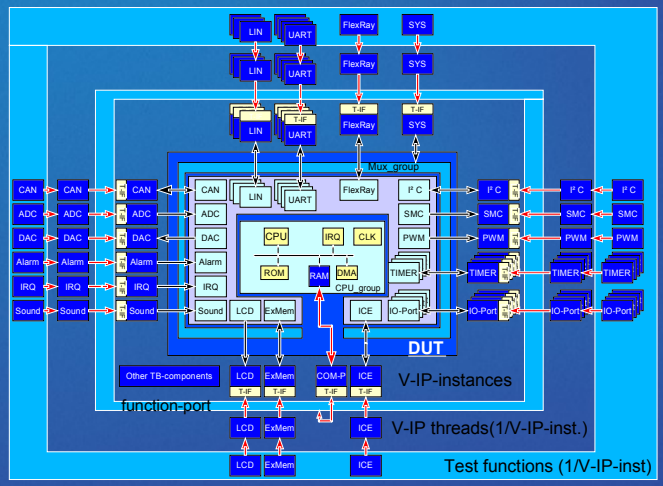
- Machine readable design specification (tables or IP-XACT compliant)
  - for IPs inside the DUT
  - for IP-interfaces
  - for the port-multiplexer
- Machine readable test specification (tables or EDA-tools like CDN-VManager)
- Machine readable coverage specification (tables or EDA-tools like CDN-VManager)
- Without standardization – Automation is impossible
  - Reuse attempts of non standardized legacy testbenches and tests may fail
  - Verification management needs to set and supervize clear rules for Verification-IP design and testbuilding



What needs to be considered technically ?

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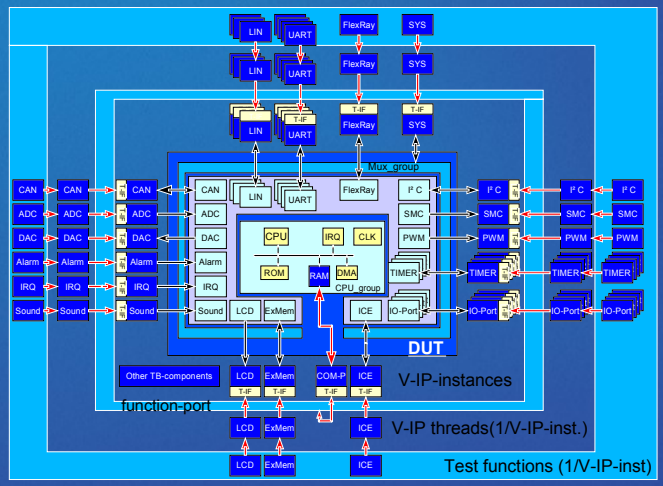
- Well defined Verification-IP architecture based on common classes for interfaces, reports and initialization.
- Verification-IPs, test functions and firmware drivers need to be self contained to allow automated testbench and test assembly.
- Try to minimize verification runtime
  - by using shortest functional testcases.
  - by using simulation models which drive and observe pins for exclusive connectivity-tests
  - Automatically replace IPs with simulation models when necessary.

- When automatic replacement of IPs is needed >>
  Well defined IP-infrastructure is mandatory
- Firmware needs to be update too >>
  Elaboration needs to report function base addresses



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